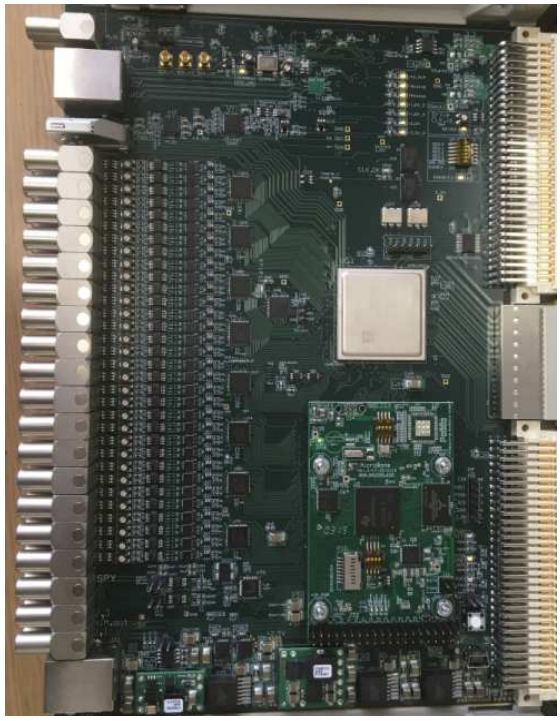
32-Channel CHK-32



CHK-32 is a compact, high performance data acquistion system. It uses a Linux Single Board Computer for control. It provides 32 digitizer channels and logic I/O for connecting to external devices. The analog inputs can be used with HPGe, silicon photomultiplers, PIN diodes, and other similar detectors.

- ADC specifications.
- Number of channels: 32.
- ADC bits: 14 (standard option) or 16 (high performance option) clocked at 100 MHz.
- ADC clock is either generated on board (default), or received over the digital interface

- Analog input specifications.
- Analog input range: 2 V with user defined offset. (E.g., +/-1 V, 0 V down to -2 V, or 0 V to +2V)
- Input connector: LEMO, compatible with standad Nuclear Physics detectors and preamplifiers.
- Input termination: 50Ω or 1 kΩ selected with a switch in each channel.
- Input polarity: both negative-going and positive-going pulses are supported.
- Baseline offsets within the ADC range are independently set for every four inputs.

- Digital I/O specifications.
- Four digital inputs and four digital outputs on the front panel.
- Either NIM or LVTTL I/O levels.
- All digital I/Os are processed in the FPGA firmware.

- Fast Waveform Synthesis DAC specifications.
- Number of DAC synthesis channels: 2.
- DAC bits: 14 at 100 MHz.
- Output range: 2V (bipolar +/- 1V).
- Arbitrary signal can be synthesized in the FPGA and output via the DAC.

- Trigger specifications.
- Independent trigger in each ADC channel.
- The trigger can be enabled/disabled independently in each ADC channel.
- Triggering on either rising or falling edge, independently selected in each channel.
- Auxiliary external trigger with front panel logic input.
- The board-level trigger is generated by OR-ing all enabled individual triggers.
- Other trigger logic firmware can be developed on request.

- FPGA specifications.
- Either XC7K325T with 1,780 kB or XC7K410T with 3,180 kB can be assembled per customer request.
- Waveform memory: up to 50,880 samples per ADC channel if all the memory is allocated to waveforms.

- Real-time DSP specifications.
- Optional signal inversion in each ADC channel.
- Optional noise suppression (i.e., signal smoothing) in each ADC channel.
- Optional trigger inversion in each ADC channel, independent from ADC inversion.

- Signal post-processing specifications.
- High performance ARM Processor can access the waveforms after every event.
- Processor specs: single core ARM Cortex A8, 1 GHz, with floating point support.
- 512 MB RAM for buffering the data and running Linux.

- Hardware interfaces.
- Two Gigabit Ethernet interfaces: one connected to the Linux computer, and the other directly to the FPGA
- UDP data streaming at full gigabit Ethernet speed, up to 118 MiBps with the direct GbE interface
- An auxiliary digital HDMI for future protocols and applications
- Remote JTAG accessible over Internet.
- VME-64 connectors are used for power.

- Embedded software.
- Debian Linux running on the Single Board Computer board.
- Embedded website with graphical waveform display in any web browser.
- Jupyter Notebook for setting up and controlling the board.
- SAMBA and NFS networking can be used to write event files directly to networked disks.
- External DAQ software not needed for evaluation because all the software is embedded.
- Site-specific readout will be developed in collaboration with the customer.
- Comprehensive and free embedded Linux development system is provided with the instrument.

- **Advantages.**
- Powerful FPGA capable of hosting comprehensive firmware.
- Trigger condition can be computed inside the FPGA in less than a microsecond.
- NIM trigger pulse can be output with the front-panel connector.
- Signal post processing can be performed by the microprocessor rather than by the FPGA. Writing the microprocessor software is significantly easier than developing the FPGA firmware.

Contact **SkuTek Instrumentation** for more information or technical questions.

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